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10/633,567	08/05/2003	Tadashi Hoshi	ASAM.0090	7171

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EXAMINER	
ENGLUND, TERRY LEE	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 04/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Terry L Englund	2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-10 and 14-18* is/are rejected.

7)☒ Claim(s) *2-4 and 11-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/081,186.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of Reference Cited (PTO-892)

DETAILED ACTION

Priority

Acknowledgment is made of the applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 10/081,186, filed on Feb 25, 2002.

Specification

The disclosure is objected to because of the following informality: The sentence added before the first paragraph of the BACKGROUND OF THE INVENTION by the Preliminary Amendment submitted on Aug 5, 2003 should be updated to indicate the application was issued as U.S. Patent 6,639,454 B2 on Oct 28, 2003. An appropriate correction is required.

Claim Objections

Claims 1-18 are objected to because of the following informalities: To improve word flow within both claims 1 and 10, it is suggested either a comma be added after "block" on line 7 within each claim, and/or the term --is-- can be added after "unit" in the same line. Since the interface circuit of claim 1 already includes a storage unit and signal gate unit, it is suggested either --further-- or --also-- be added prior to "includes" on line 2 of claim 4. It is suggested "provide" on line 6 of both claims 6 and 15 be changed to --provided-- to improve word flow. One of the excess periods at the end of claim 11 should be deleted. Similar to claim 4 above, it is suggested either --further-- or --also-- be added prior to "includes" on line 2 of claim 13. Claim 13, line 6 "or" should be --of--, and line 11 "Mock" should to --block--, to correct inadvertent oversights. Appropriate corrections are required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 5-9, and 14-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. Claim 6, lines 3-4 "a power supply line...is provided in the power supply line" is confusing. For example, was "provided in the power supply line" meant to be --provided in the third area--? Since each of claims 6 and 17 ends with a comma, it is not clear if any additional limitation was intended to be recited. If not, the comma must be changed to a period because the claims appear to be incomplete as presently written. Claim 15, lines 4-5 have the same "power supply line...provided in the power supply line" type problem as claim 6 described above.

Claim 5 recites the limitation "the interface circuit block" in lines 5-6. There is insufficient antecedent basis for this limitation in the claim. Was --the interface circuit-- meant, or is "the interface circuit block" somehow different from it?

Claim 7 recites the limitation "the second circuit" in line 3 with insufficient antecedent basis for this limitation in the claim. If it is meant to refer back to the "second circuit block" of claim 1, then consistent labeling would minimize confusion.

Claim 14 recites the limitation "the interface circuit block" in lines 5-6. There is insufficient antecedent basis for this limitation in the claim. Was --the interface circuit-- meant, or is "the interface circuit block" somehow different from it?

Claim 16 recites the limitation "the second circuit" in line 3 with insufficient antecedent basis for this limitation in the claim. If it is meant to refer back to the "second circuit block" of claim 10, then consistent labeling would minimize confusion.

Dependent claims carry over any rejection(s) from any claim(s) upon which they depend.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 5 and 14 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,639,454. Although the conflicting claims are not identical, they are not patentably distinct from each other because the first/second circuit blocks, interface circuit with storage unit and signal gate unit, first supply voltage, and first/second areas of the present application's claims 5 and 14 correspond to the patent's plurality of circuit blocks, interblock interface circuit with storage means and signal gate means, power source voltage, and area/surface, respectively. For example, one of ordinary skill in the art would recognize the present application's "the first supply voltage is stopped to apply to the first circuit block in the second mode" corresponds to when "a supply of power source

at least one circuit block" recited within the patent's claim 1. Similarly, the present application's "a storage unit to hold a state of the output of the first circuit block" and "the signal gate unit disconnects the storage unit from the output of the first circuit block" correspond to the patent's claim 1 "storage means for storing therein a state of said signal" and "signal gate means for preventing transmission of a signal output from at least one...blocks."

Claims 1 and 10 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 2 and/or claim 3 of U.S. Patent No. 6,639,454. Although the conflicting claims are not identical, they are not patentably distinct from each other because these claims are obvious type variations of the claims recited within the patent (e.g. see the previous description with respect to the application's claims 5 and 14 versus claim 1 of the patent. The major difference between these claims appears to be the lack of a control circuit within the present application's independent claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 7, 10, and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Ooishi. Fig. 4 shows a semiconductor integrated circuit device comprising first circuit block 22 having first/second modes (e.g. see NORMAL/SLEEP in Fig. 5); second circuit block 25; and

of second circuit block 25. Interface circuit 23,24 includes storage unit 24 for basically holding a state of the first circuit block's output (e.g. see the Abstract, and Fig. 5's SLEEP MODE with respect to signals D5,/D5, and signals D3,/D3 transitioning between the NORMAL and SLEEP modes). The interface circuit also includes signal gate unit 23 provided between storage unit 24 and first circuit block 22. In the first (NORMAL) mode, first supply voltage VCC (PS0) is applied to first circuit block 22 (e.g. see Fig. 5), and in the second mode, first supply voltage VCC is stopped from being applied to first circuit block 22 since PS0 has been switched to GND (e.g. see Fig. 5). In the first (NORMAL) mode, and as long as control signal TG2 is high, signal gate unit 23 connects storage unit 24 to output D3,/D3 of first circuit block 22, and in the second (SLEEP) mode, signal gate unit 23 disconnects storage unit 24 from the first circuit block's output D3,/D3, thus anticipating claim 1. Since second power supply voltage PS1 is applied to interface circuit 24, and third power supply voltage VCCC is applied to second circuit (block) 25, claim 7 is also anticipated. Interpreting Ooishi's circuit in a slightly different manner, signal gate unit 23 connects storage unit 24 to output D3,/D3 of first circuit block 22 when first power supply VCC (PS0) is applied to first circuit block 22 and control signal TG2 is high; wherein signal gate unit 23 disconnects storage unit 24 from output D3,/D3 of first circuit block 22 when first power supply VCC is stopped being applied to first circuit block 22 (e.g. see the SLEEP MODE in Fig. 5). Therefore, claim 10 is anticipated. For the same reasoning as applied to claim 7 above, claim 16 is anticipated.

[Note: To overcome the above prior art rejections with respect to Ooishi, it is suggested the operation of the claimed signal gate unit be amended. For example, claims 1 (lines 12-13) and 10 (lines 9-10) could be modified to indicate the storage unit is continuously connected to

the first circuit block's output by the signal gate unit (when in the first mode as recited within claim 1, or when the first power supply is applied as recited within claim 10). The reference of Ooishi only connects them according to transfer clock TG2, which intermittently connects and disconnects 24 and 22 in the NORMAL MODE (e.g. see Fig. 5).]

No claim is allowable as presently written.

Allowable Subject Matter

However, claims 2-4, and 11-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. There is presently no strong motivation to motivation to modify or combine any prior art reference(s) to ensure the first circuit block includes a plurality of registers are recited within claims 2 (upon which claims 3 and 4 depend) and 11 (upon which claims 12 and 13 depend).

Claims 6, 8, 9, 15, 17, and 18 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. There is presently no strong motivation to modify or combine any prior art reference(s) to ensure the device has: 1) a third area as recited within claims 6 and 15; and 2) the first-third power supply voltages as recited within each of claims 8, 9, 17, and 18.

Also, claims 5 and 14 would be allowable if their respective double patenting rejections, and their rejections under 35 U.S.C. 112, second paragraph. There's presently no strong motivation to modify or combine any prior art reference(s) to ensure the device includes the separated first and second areas as recited within claims 5 and 14.

Prior Art

The other prior art reference cited on the accompanying PTO-892 is deemed relevant to at least sections of the claimed limitations, but it is only cited for interest and documentation purposes. Coughlin, Jr. et al. shows a circuit in the sole figure that comprises first/second circuit blocks 12/16 both having first and second modes (e.g. in one mode, first supply voltage VDD 22 is applied to circuit blocks 12/16; and in another mode, first supply voltage VDD 22 is turned off (or stopped from being applied to circuit blocks 12/16; see column 2, lines 35-51), wherein what can be deemed an interface circuit 14 is coupled between output DC,DCN of first circuit block 12 and input L1,L1N of second circuit block 16. Interface circuit 14 holds the state of the data within the circuit (e.g. see column 2, lines 49-51). However, even if T9 and T11 of interface circuit 14 are deemed one type of signal gate unit, and T12-T15 are deemed a storage unit, the reference was filed Mar 27, 2002, which is after the filing date of the present application's parent application (i.e. 10/081,186 was filed Feb 25, 2002). Therefore, the reference of Coughlin, Jr. et al. does not meet the prior art criteria with respect to this case.

The prior art references cited on the IDS submitted Aug 5, 2003 were reviewed and considered. None of these references clearly show or disclose the first/second circuit blocks, and the interface circuit with a storage unit and signal gate unit, as recited within the independent claims.

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

TLE

Terry L. Englund

18 April 2004

TIMOTHY P. CALLAHAN
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